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Design of STT-RAM cell in 45nm hybrid CMOS/MTJ process

Karrar Hussain
CVR College of Engineering
Andhra Pradesh, India

Dr. C V Krishna Reddy
NNRES
Andhra Pradesh, India

Dr. K Lal Kishore
JNTU - Anantapur
Andhra Pradesh, India

Abstract: This paper evaluates the performance of Spin-Torque Transfer Random Access Memory (STT-RAM) basic memory cell configurations in 45nm hybrid CMOS/MTJ process. Switching speed and current drawn by the cells have been calculated and compared. Cell design has been done using cadence tools. The results obtained show good agreement with theoretical results.

Keywords: STT-RAM, Magnetic Tunnel Junction (MTJ), Perpendicular Magnetic Anisotropy (PMA), Hybrid CMOS/MTJ process.

1. INTRODUCTION

STT-RAM is an emerging nonvolatile memory that has all the characteristics of a universal memory. It is nonvolatile, highly scalable, has low power consumption, unlimited endurance, high density and multilevel cell capability. In this paper preliminary investigations of switching speed and current capabilities of the basic STT-RAM memory cells for two different models i.e. In-plane and perpendicular magnetic anisotropy (PMA) has been done. The cell design is done using cadence tools in 45nm hybrid CMOS/MTJ process. The results show that the performance of STT-RAM cells is comparable to that of theoretical results.

2. STT-RAM TECHNOLOGY

The development of spintronics was due to the discovery of giant magnetoresistance (GMR) by [1, 2]. The main principle in spintronics is the manipulation of spin-polarized currents in contrast to traditional electronics where spin is ignored. As first suggested by Mott [3] spin-polarized currents can be generated by exploiting the influence of the spin on the transport properties of the electrons in ferromagnetic conductors. The discovery of tunneling magnetoresistance (TMR) followed the GMR. The important milestone was reached when S. Yuasa et al.[4] and Parkin et al. [5] showed that very large TMR ratios up to 200% at room temperature could be obtained with MgO Magnetic Tunnel Junction (MTJ).

The main element of the STT-RAM is the MTJ cell. The MTJ consists of two ferromagnetic layers separated by a barrier layer made of MgO as shown in figure 1. The MTJ resistance is determined by the relative magnetization directions of the two ferromagnetic layers. When the magnetization directions of the layers are parallel, the MTJ is in low resistance state (representing a bit 0), whereas if the layers are antiparallel, the MTJ is said to be in high resistance state (representing a bit 1). Data storage is realized by switching the MTJ between high and low resistance states. [7]

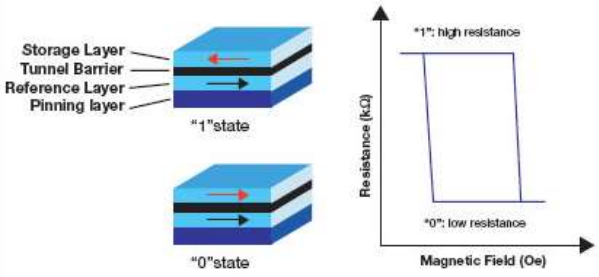

Figure 1. MTJ structure representing antiparallel ('1' state) and parallel ('0' state) [Alexander Driskill et al, Grandis corporation]

3. BASIC STRUCTURE OF STT-RAM MEMORY CELL

The basic structure uses an MTJ as the storage element and a N-channel MOSFET (1T-1MTJ) as the selection device.[8] Figure 2 shows the diagrams of the circuit and cross section of the structure. In the STT-RAM cell the source of the NMOS transistor is connected to the source line (SL). The free layer of the MTJ is connected to the bit line (BL) while the other pinned layer to the drain of NMOS. The word line (WL) is connected to the gate. In this arrangement the STT-RAM uses existing CMOS technology with additional 2-3 masks only.

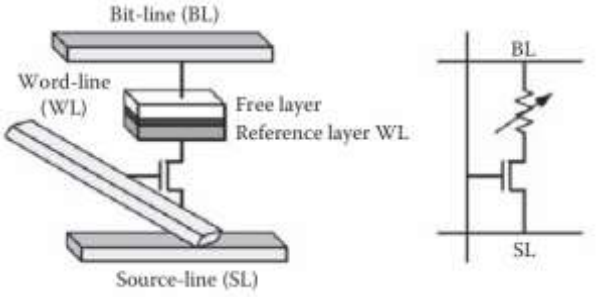

Figure 2. 1T-1MTJ STT-RAM (a) cross section and (b) circuit diagram

3.1 Read and Write Mechanisms

The switching of the states in MTJ is obtained by changing the direction of current through it. When writing '0' the current flows from BL to SL, whereas when writing '1' the current flows in opposite direction i.e from SL to BL. when the MTJ terminal is biased to VDD, the cell access transistor operates in the linear region and does not limit the current through the MTJ. Therefore a resistor is connected to limit the current through it. In the reverse bias case, the access transistor operates in a diode connected manner and thus the threshold drop across the access device limits the voltage drop across the MTJ. This voltage drop places an upper limit on the switching current that can be applied to the cell.

The data read operation is slightly different from that of conventional memory cell. The STT-RAM requires a reference voltage to compare the output generated by the sense amplifier. Generally the reference voltage is chosen as the voltage drop across the resistance $(R_L + R_H) / 2$ where R_L and R_H are the resistances of MTJ in parallel and anti-parallel states respectively. The read operation consists of making the word line as high, this selects the access transistor. By applying a read voltage to the selected memory cell, the generated current on the bit line can now be compared to the reference signal in the sense amplifier.

4. STT-RAM TECHNOLOGIES

There are two types of switching mechanisms in STT-RAM currently, the In-plane switching (IPS) and the perpendicular magnetic anisotropy (PMA) type. The PMA are advantageous over IPS anisotropy type for reducing switching current density in MTJ's. Devices with IPS magnetic anisotropy materials have to overcome additional demagnetizing fields. So STT-RAM devices with PMA are attracting much interest for STT-RAM applications. Perpendicular MTJ's with Tunnel magneto resistance (TMR) ratios up to 64% at room temperature are reported using rare earth transition metal alloys [9][10].

5. STT-RAM CELL DESIGNS

In addition to the one transistor-one MTJ (1T-1MTJ) structure shown in Figure 2 several other cell designs like two transistor-one-MTJ (2T-1MTJ) [11] and thermally assisted MRAM (TAS-RAM) also exist. [12] The 1T-1MTJ cell has the advantage of less area but it is vulnerable to process variations and thus cell stability is less. J. Li et al [11] proposed the 2T-1MTJ cell model which is more robust to process variations. This model compensates cell instability during read operations and improves write operation by sacrificing the area. Therefore memory density is less compared to 1T-1MTJ cell.

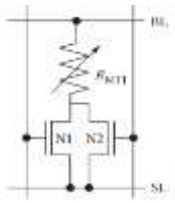

Figure 3. 2T-1MTJ STT-RAM cell

The 2T-1MTJ cell consists of two NMOS transistors, one for read (N1) and the other for write operation (N2) as shown in figure 3. During the read operation only the read NMOS is turned on whereas during write operation both the read and write NMOS are turned on to provide large current for better write stability. This technique provides more robustness than the 1T-1MTJ cell. However the cell area increases due to the two transistors.

6. SIMULATION RESULTS

In our work we have used the two types of STT-RAM models i.e IPS and PMA type and designed the basic memory cells as mentioned in the previous section. The design has been carried out in 45nm technology using cadence tools and simulation results have been obtained. The results are as follows: Figure 4 (a) shows the schematic of IPS 1T-1MTJ cell and Figure 4(b) its simulation outputs. Figure 5(a) and 5(b) shows the 1T-1MTJ results obtained using PMA model.

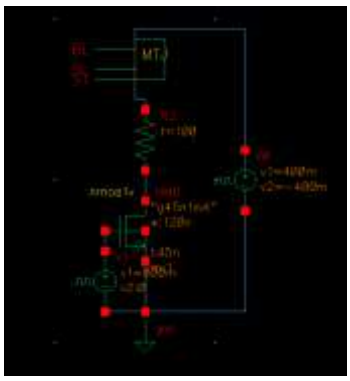

Figure 4(a) : Schematic of 1T-1MTJ cell (IPS)

Figure 4(b) : Outputs of 1T-1MTJ cell (IPS)

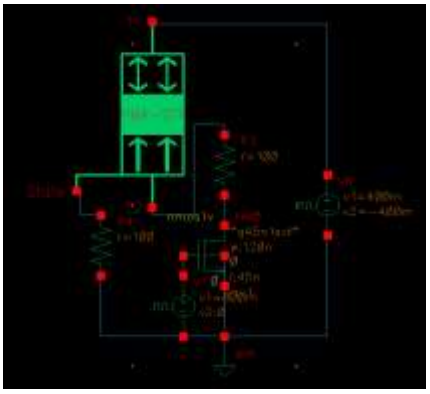

Figure 5(a) : Schematic of 1T-1MTJ cell (PMA)

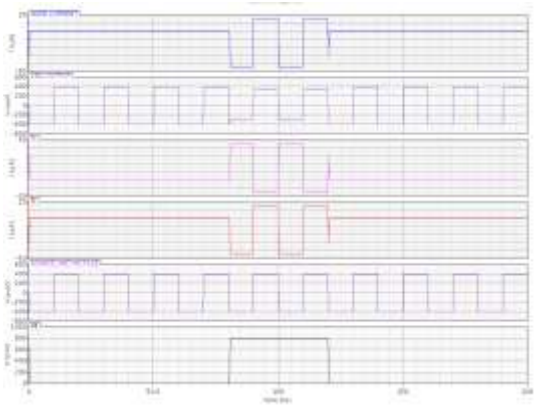

Figure 5(b) : Outputs of 1T-1MTJ cell (PMA)

Similarly, Figure 6(a) and (b) respectively shows the schematic and simulation outputs of 2T-1MTJ IPS type and finally Figure 7(a) and (b) the schematic and outputs of 2T-1MTJ for PMA model.

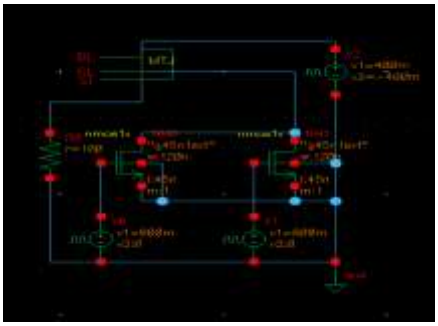

Figure 6(a) : Schematic of 2T-1MTJ cell (IPS)

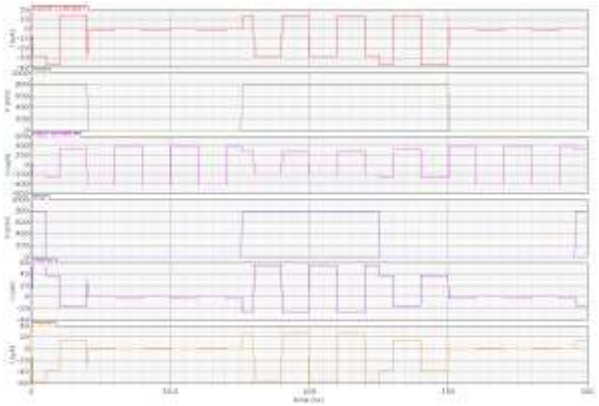

Figure 6(b) : Outputs of 2T-1MTJ cell (IPS)

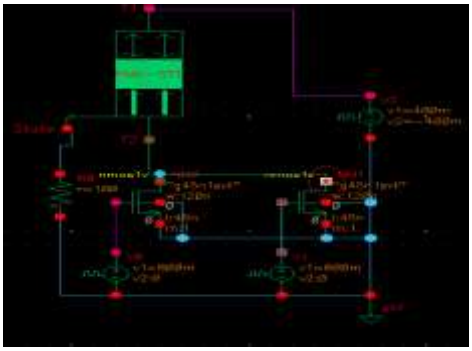

Figure 7(a) : Schematic of 2T-1MTJ cell (PMA)

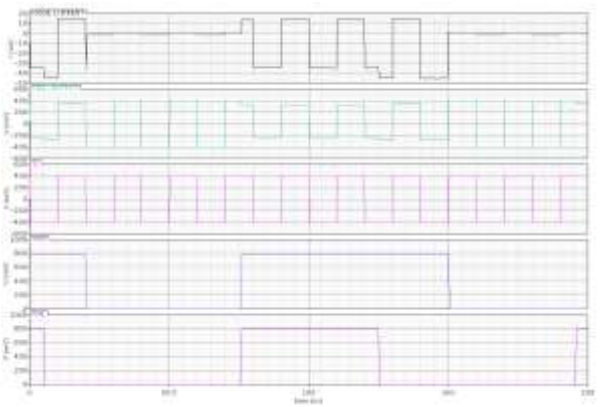

Figure 7(b) : Outputs of 2T-1MTJ cell (PMA)

7. CONCLUSIONS

In this paper, design of basic STT-RAM memory cells has been carried out in 45nm technology node. Two types of models have been used, the IPS and the PMA type. Using these models we have designed two types of memory cells i.e the 1T-1MTJ and 2T-1MTJ type. The results show that the write current for IPS 1T-1MTJ is approx. 35μA and for PMA type it is around 30 μA. Similarly the write current for 2T-1MTJ of PMA type is approx. 50 μA compared to 55 μA drawn by IPS type.

The results clearly show that the write current for PMA type is less when compared to IPS type for both the memory cells. However, the switching speed of both types are nearly the same.

8. ACKNOWLEDGMENTS

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