Digitally controlled boost PFC converter

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Abstract. The goal of the paper developing a fully digital control for a boost power factor preregulator
• Exploiting the potentialities of digital control to To compensate the digital delay computation approach controller improve the system's dynamic performance

Keywords: Boost converter, digital controller, power factor correction, voltage compensator, current compensator

1. INTRODUCTION

Applications of digital controllers are becoming more and more widespread in power electronic converters. In the low-to medium power application, when the price of the controller cannot be compensated by the performance, the major drawback is the sample and hold time considered as delay introduced by a digital controller, which is minimized by high sampling frequency.

Recent publications [6-12] demonstrate that purely digitally controlled PFCs are feasible and exhibit a number of benefits such as flexibility and programmability, decreased number of active and passive components, and, as a consequence, improved reliability, negligible and or compensatable offsets and thermal drifts. Additionally, digital control offers the potential of implementing sophisticated adaptive and nonlinear control methods to improve stationary and dynamic performance and to implement power management strategies to improve efficiency. However, the current control loop has to provide a much higher bandwidth than the voltage control loop. Therefore, high computing power and costly DSP would be needed if going fully digital. Even fully digital control still needs some analog circuits for time-critical safety shutdown or shunt signal amplification. Digital control is the trend for tomorrow's DC power supply systems. Despite the merits of communication ability, noise immunity and capability to implement complex control methods. Digital control has its disadvantages. DPWM resolution and digital delay is the bottleneck in implementing digital control for PFC. It is necessary to know the requirement for ADC resolution, DPWM resolution and the system clock.

The paper presents the effect of digital delay and how it influences the performance of PFC are studied. The compensation method is proposed to improve PF with low current loop gain design. Simulation results are presented to prove the effectiveness of this solution.
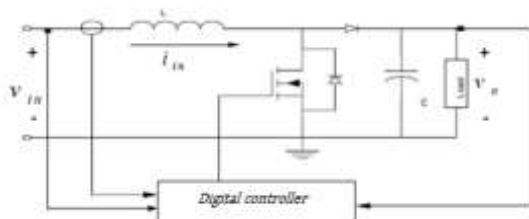

Figure. 1. Digitally controlled boost converter

2. PFC BOOST CONVERTER

Among the three basic power converters-buck, boost, buck-boost-the boost converter is the most suitable for use in implementing PFC. Because the boost inductor is in series with the line input terminal, the inductor will achieve smaller current ripple and it is easier to implement average current mode control. Buck converter has discontinuous input current and would lose control when input voltage is lower than the output voltage. The buck-boost converter can achieve average input line current, but it has higher voltage and current stress, so it is usually used for low-power application [17]. The power stage adopted in this paper is boost converter operating in continuous conduction mode. Figure 2 shows the circuit diagram of the boost PFC converter [17].
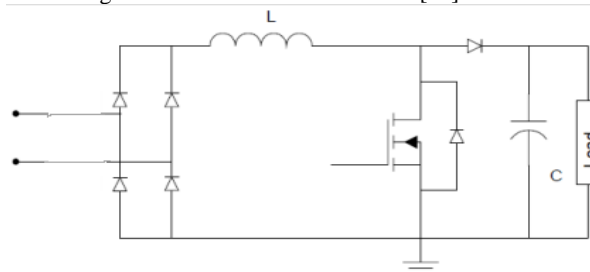

Figure 2. Boost converter

3. CURRENT LOOP COMPENSATION MODEL

The function of the current compensator is to force the current to track the current reference that is given by the multiplier and which has the same shape as the input voltage. So the current loop bandwidth must be higher than the reference bandwidth. For faithfully tracking a semi-sinusoidal waveform of 100Hz, the bandwidth of the current loop is usually set to 2-10 KHz [16]. Using the three terminal average models, a small-signal equivalent circuit of the current loop is shown in Figure 3.
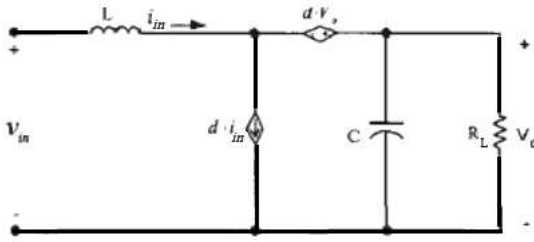
Figure 3 .Average equivalent circuit model of Boost topology

The power stage small-signal duty-to-current transfer function is derived as follows [16]:

$$G_{id} = \frac{\tilde{i}_{in}}{\tilde{d}} = \frac{2V_o}{R_L(1-D)^2} \frac{1+\frac{sR_LC}{2}}{1+\frac{sL}{R_L(1-D)^2}+\frac{s^2LC}{(1-D)^2}} \qquad (1)$$

For $s = j\omega$, when large enough, the high frequency approximation is can be derived:

$$G_{id} = \frac{\tilde{i}_{in}}{\tilde{d}} \approx \frac{V_o}{Ls} \qquad (2)$$

A small-signal discrete-time relation yields the control-to current Transfer function:

$$G_{idz}(z) = \frac{\tilde{i}_{in}(z)}{\tilde{d}(z)} = \frac{Vo}{L}\frac{T_s}{(z-1)} \qquad (3)$$

Where V_C, V_{in}, V_o are steady state value and $\tilde{v}_{in}\tilde{v}_c$ $\tilde{v}_o$ are small signal perturbations.

4. VOLTAGE LOOP COMPENSATION

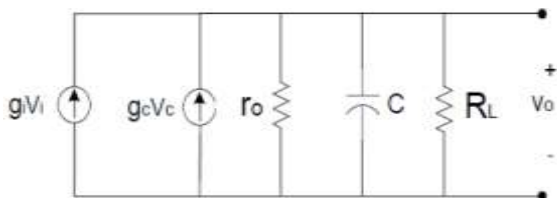Then, a low-frequency small-signal model is developed to design voltage Compensator, as shown in Figure 4.

Figure 4 . low-frequency Small-Signal Model for voltage loop

$$g_c = k\frac{V_{in\ rms}}{V_o} \qquad (4)$$

$$g_i = k\frac{2\,V_{in}\,V_c}{V_o} \qquad (5)$$

and

$$r_o = \frac{V_o}{I_o} \qquad (6)$$

For a constant power load, we have

$$R_L = -\frac{V_o}{I_o} \qquad (7)$$

[16]. from the small-signal model, the control to output voltage transfer function is derived as follows:

$$G_v = \frac{\tilde{v}_o}{\tilde{v}_c} = \frac{g_c}{Cs} \qquad (8)$$

For a constant power load, a voltage compensation of 45° phase margin is adopted [16].

5. PULSE WIDTH MODULATION RESOLUTION

Digital PWM resolution is closely related to the system clock. For a digital PWM whose operation is based on the system clock, the resolution is

$$R = \frac{f_{switch}}{f_{clock}} \qquad (9)$$

$$|w_{pwm}(jw)| \approx \frac{R}{2}\cdot\frac{4}{\pi} \qquad (10)$$

Based on this approximation and some specific conditions in a certain control system, adequate resolution can be calculated.

6. DIGITAL DELAY

The sample and hold of continuous signals and the non-zero computation time cause delay in a digital control system. Delay in a system usually causes phase lag that leads to reduction of the phase margin.
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7. COMPUTATION DELAY

The computation delay can be expressed as

$$D_{delay} = e^{-s.T_{delay}} \qquad (11)$$

Because in a PFC converter the fastest loop is the current loop, the digital delay affects the current loop most. Assuming the controller has one switching cycle or 10μs delay for ADC, PWM and computation, there is 29° phase shift reducing the phase margin by the same volume (shown in Figure 5). This delay has to be compensated to stabilize the system. It is predictable that compensating this delay will result in a poor current compensator performance. Its exact influence and compensation will be further.

Alternatively, we design the digital controller directly in z-domain employing the relation of z variable and s variable:

$$z = e^{sT_s} \qquad (12)$$

Where Ts is the sampling cycle

These responses are directly related to the position of zeros and poles on the z plain Particularly, the computation delay $T_{delay}=10\mu s$

$$e^{-T_{delay}s} \qquad (13)$$

Can be mapped into the origin as s
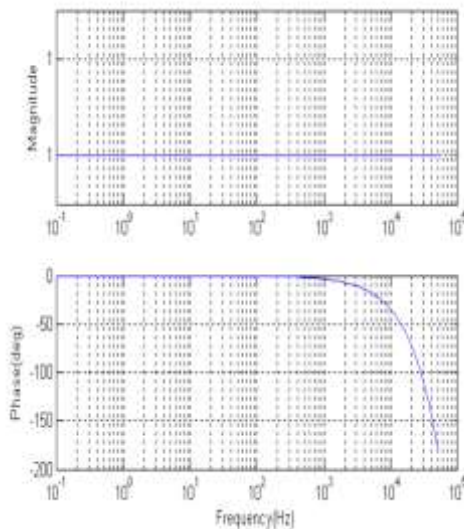
$$z^{-\frac{T_{delay}}{T_s}} \qquad (14)$$
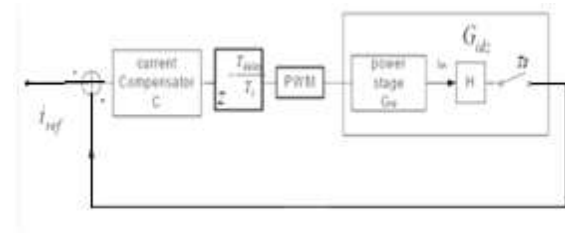
Figure 5 .Effect of digital delay

Figure 6.Current loop with digital compensator

The design target is similar to that of the analog compensator. For robustness, the phase margin is set to 45°. For a faithful tracking of the semi sinusoidal Waveform, the bandwidth is w_c =8 KHz. To compensate the digital delay the one-zero approach, in which the zero is moved toward the origin.

10. ONE-ZERO APPROACH

The current compensator is

$$C(z) = K_p \frac{z-\alpha}{z-1} \quad (15)$$

$$T_c = C(z)G_{idz}z^{-\frac{T_{delay}}{T_s}} \quad (16)$$

The two design targets, crossover frequency and phase margin are used to determine two unknown variables, gain K_P and zero, as follows:

$$\begin{cases} |T_c \, e^{jw_cT_s}| = 1 \\ \angle T_c \, e^{jw_cT_s} = -180° + 45° \end{cases} \quad (17)$$

By solving Equation 17, the value of gain K_P and zero α are obtained:

K_P=0.0036

α=1.44

11. VOLTAGE LOOP COMPENSATOR

The discrete transfer function of the voltage compensator can be expressed as

$$G_{cv}(z) = \frac{K_{pv}}{z-\rho} \quad (18)$$

$$g_c = k\frac{Vin^2}{V_0} \quad (19)$$

From the given parameters, we can calculate that $g_c = 1.45$. Hence the discrete
Control-to-voltage transfer function is:

$$G_v(z) = \frac{g_c}{C} \cdot \frac{T_s}{z-1} \quad (20)$$

The voltage open loop gain is:

$$T_v = G_{cv}(z)G_v(z)z^{-\frac{T_{delay}}{T_s}} \quad (22)$$

Since the voltage compensator gain at low frequencies is flat, the crossover frequency of voltage loop can be determined from

8. DISCRETIZATION OF THE CONTROLLERS

• Since the control bandwidths are sufficiently low, as compared to the sampling frequency, it is possible to use a simple discretization method, without an excessive frequency response distortion.
• In this case Euler integration method was used.
• This uses the following Z-form, where Ts is the sampling period:

$$s = \frac{1 - z^{-1}}{T_s}$$

It is worth noting that, in these conditions, the use of different discretization techniques, such as the trapezoidal Z-form, only implies a small variation of the controllers' gains.
• It is also worth noting that the rectangular (Euler) Z-form maintains the proportional gain and only modifies the integral gain (it is multiplied by Ts).

9. CURRENT LOOP COMPENSATOR

As mentioned before analog low-pass filters with cutoff frequency equal to half of the switching frequency are inserted in the current and voltage feedback loops in order to reduce the aliasing effect. As a result, only the frequency range below
half of the switching frequency is of concern in digital controller design and the transfer function of the low pass filter is ignored. When we are designing the current compensator, the influence of slow voltage loop can be ignored. The current loop with digital compensator is illustrated in Figure 6
The current loop gain is:

$$G_{cv}(100Hz) = G_{cv}(f_c) \qquad (23)$$

Thus, the bandwidth of the voltage loop is chosen to be 10~20Hz.

Thus we have two variables: the poles for voltage compensator ρ, and the gain of voltage compensator K_{pv}, so where

$$\begin{cases} |T_v \, e^{jw_cT_s}| = 1 \\ < T_v \, e^{jw_cT_s} = -180° + 45° \end{cases} \qquad (24)$$

From Equation 24, voltage compensator parameters are found:

$$K_{pv} = 0.0017$$

$$\rho = 1.$$

12. SIMULATION RESULTS

The current control methods have been developed and implemented on the MATLAB/SIMULNK programming environment. The purpose of this simulation is to show the effectiveness for PFC circuit and in reducing the supply current harmonic distortion.

Power Stage Parameters

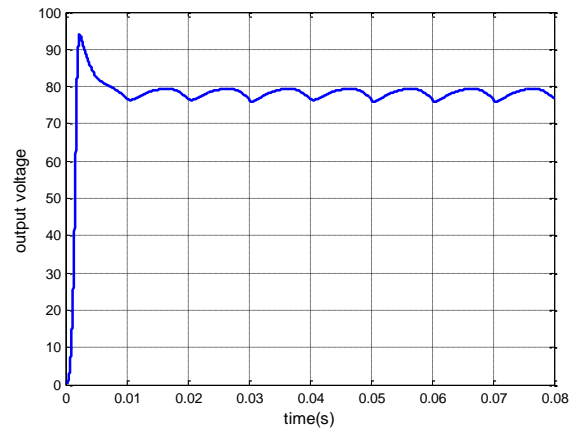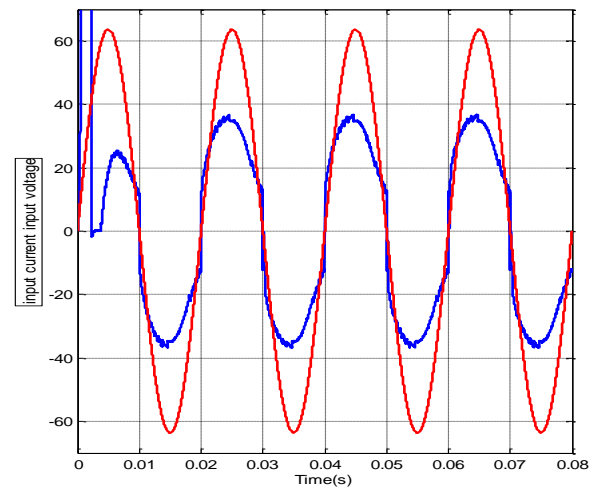| Paramèters	Boost Converter
Input voltage V_{in}	45 V
Output voltage V_0	80V
Inductance L	1mH
Capacitor C	440 µF
load R_L	100Ω
Switching frequency	$f_s = 100kHz$

Figure.7 Output voltage

Figure.8 Wave form input current and voltage Vo red I_{in} blue

13. CONCLUSIONS

This paper presents a discrete control for the boost power factor corrected rectifier. Simple linearized discrete models for both the current loop and for the voltage loop have been derived, Simulation is performed by using MATLAB to verify the proposed digital PFC controller..To compensate for the computational delay, a one zero approach controller has been successfully designed.

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